In the Claims:

Please cancel claims 4-7, 9, 11-12, 16-19, 21, and 23-26. Claims 1 and 13 have been Amended. The claims are as follows:

1. (Currently Amended) A phase lock loop circuit, comprising:

a first charge pump circuit, a second charge pump circuit, and a loop filter circuit within the phase lock loop circuit, the first charge pump circuit comprising a first adjustable gain ~~control~~, the second charge pump circuit comprising a second adjustable gain ~~control~~, the loop filter circuit comprising a filter capacitor with a constant capacitance value C, the first charge pump circuit being electrically connected to the loop filter circuit, ~~the first charge pump circuit being adapted to control a flow of current for the loop filter, the loop filter being adapted to provide a voltage for a voltage controlled oscillator~~, the second charge pump circuit being electrically connected to the loop filter circuit in parallel with the filter capacitor, ~~and the first charge pump circuit and the second charge pump circuit being adapted to collectively vary an effective capacitance value of the filter capacitor.~~ the first charge pump circuit being adapted to source a first current to said loop filter circuit, the second charge pump circuit being adapted to source a second current to said loop filter circuit, the first charge pump circuit and the second charge pump circuit being adapted to collectively decrease an effective capacitance value C_{eff} of the filter capacitor by adjusting said first adjusable gain to a first gain value G_m and said second adjustable gain to a second gain valueG_o, the effective capacitance value C_{eff} being determined by an equation $C_{eff} = (C^* G_m)/(G_m+G_o)$, and the loop filter being adapted to provide a voltage for a voltage controlled oscillator.

2. (Original) The phase lock loop circuit of claim 1, wherein the first charge pump circuit and the second charge pump circuit are further adapted to collectively vary a bandwidth of the phase lock loop circuit.

3. (Original) The phase lock loop circuit of claim 1, wherein the first charge pump circuit and the second charge pump circuit are further adapted to collectively vary a damping factor of the phase lock loop circuit.

4-7. (Canceled)

8. (Original) The phase lock loop circuit of claim 1, wherein the first charge pump circuit and second charge pump circuit are further adapted to collectively reduce noise signals from an output signal of the phase lock loop circuit.

9. (Canceled)

10. (Original) The phase lock loop circuit of claim 1, wherein the first charge pump circuit and the second charge pump circuit are further adapted to collectively vary a bandwidth and a damping factor of the phase lock loop circuit simultaneously.

11-12. (Canceled)

13. (Currently Amended) A method for optimizing a phase lock loop circuit, comprising:

providing a first charge pump circuit, a second charge pump circuit, and a loop filter circuit within the phase lock loop circuit, the first charge pump circuit comprising a first adjustable gain ~~control~~, the second charge pump circuit comprising a second adjustable gain control, the loop filter circuit comprising a filter capacitor with a constant capacitance value C, the first charge pump circuit being electrically connected to the loop filter, and the second charge pump circuit being electrically connected to the loop filter circuit in parallel with the filter capacitor;

~~controlling, by the first charge pump circuit, a flow of current for the loop filter;~~

sourcing by the first charge pump circuit, a first current to said loop filter circuit;

sourcing by the second charge pump circuit, a second current to said loop filter circuit;

~~varying, by the first the first charge pump circuit and the second charge pump circuit, an effective capacitance value of the filter capacitor; and~~

decreasing an effective capacitance value C_{eff} of the filter capacitor by adjusting said first adjusable gain to a first gain value G_m and said second adjustable gain to a second gain valueG_m, wherein the effective capacitance value C_{eff} is determined by an equation $C_{eff} = (C^* G_m)/(G_m+G_o)$; and

providing, by the loop filter, a voltage for a voltage controlled oscillator.

14. (Original) The method of claim 13, further comprising varying, by the first the first charge pump circuit and the second charge pump circuit, a bandwidth of the phase lock loop circuit.

15. (Original) The method of claim 13, further comprising varying, by the first the first charge pump circuit and the second charge pump circuit, a damping factor of the phase lock loop circuit.

16-19 (Canceled)

20. (Original) The method of claim 13, further comprising reducing, by the first the first charge pump circuit and the second charge pump circuit, noise signals from an output signal of the phase lock loop circuit.

21. (Canceled)

22. (Original) The method of claim 13, further comprising varying, by the first charge pump circuit and the second charge pump circuit, a bandwidth and a damping factor of the phase lock loop circuit simultaneously.

23-26. (Canceled)